

## EAST SEARCH

6/24/04

L#	Hits	Search String	Databases	
L1	14342	((microprocessor or microcomputer or CPU or (processing adj unit)) with (power near2 (circuit\$1 USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB		
L2	14404	((microprocessor or microcomputer or CPU or (processing adj unit)) with (power near2 (circuit\$1 USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB		
L3	1243	((microprocessor or microcomputer or CPU or (processing adj unit)) with (power near2 (circuit\$1 USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB		
L4	43	((microprocessor or microcomputer or CPU or (processing adj unit)) with (power near2 (circuit\$1 USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB		
L5	24	((microprocessor or microcomputer or CPU or (processing adj unit)) with (power near2 (circuit\$1 USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB		
L6	3	((microprocessor or microcomputer or CPU or (processing adj unit)) with (power near2 (circuit\$1 USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB		
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L12	64	((microprocessor or microcomputer or CPU or (processing adj unit)) with (power near2 (circuit\$1 USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB		
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L14	6	((microprocessor or microcomputer or CPU or (processing adj unit)) with (power near2 (circuit\$1 USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB		
L15	6	((microprocessor or microcomputer or CPU or (processing adj unit)) with (power near2 (circuit\$1 USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB		
L16	63	((microprocessor or microcomputer or CPU or (processing adj unit)) with (power near2 (circuit\$1 USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB		
L17	17	(anti-resonance near2 (circuit\$1 or system\$1))		
L18	166	anti-resonance with (model\$3 or simulat\$3)		
L19	21	anti-resonance with filter\$1		
L20	59625	(resonance or resonant) with circuit\$1 and simulat\$3		
L21	265	(resonance or resonant) with circuit\$1 with simulat\$3		
L22	6	((resonance or resonant) with circuit\$1 with simulat\$3 and "leading edge"		
L23	15	((resonance or resonant) with circuit\$1 with simulat\$3 and (clock adj (signal or cycle))		
L24	2	((resonance or resonant) with circuit\$1 with simulat\$3 and (simulat\$3 with (clock adj (signal or cycle))		
L25	7	((microprocessor or microcomputer or CPU or (processing adj unit)) with (power near2 (circuit\$1 USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB		
L26	5	((resonance or resonant) with circuit\$1 with simulat\$3 and (resistor\$1 with "voltage controlle		
L27	1	((resonance or resonant) with circuit\$1 and (circuit\$1 with simulat\$3 with "leading edge")		
L28	1	((resonance or resonant) with circuit\$1 and (simulat\$3 with "leading edge")		
L29	4	("integrated circuit" or "power model") with "transistor description"		
L30	30	(transistor near2 model\$1) with ((resistance or resistor) near2 model\$1) with ((capacitance or		
L31	2	(transistor near2 model\$1) with ((resistance or resistor) near2 model\$1) with ((capacitance or		
L32	2	((transistor near2 model\$1) with ((resistance or resistor) near2 model\$1) with ((capacitance or		
L33	5	transistor description with (format or model)		

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Results of search set L24:(transistor near2 model\$1) with ((resistance or resistor) near2 model\$1) with ((capacitance or capacitor) near (anti-resonance near2 (circuit\$1 or system\$1))) model\$1)

Document Kind	Codes	Title	Issue Date	Current OR	Abstract
US 20030200071 A1		Simulation method	20031023	703/15	
US 200307169059 A1		Method and program product for evaluating a circuit	20030911	324/713	
US 20030139164 A1		Fixed termination scheme for differential receiver that compensates for process, voltage, and	20030724	455/282	
US 20030030480 A1		Low noise analog multiplier utilizing nonlinear local feedback elements	20030213	327/359	
US 20020157069 A1		Method and apparatus for preparing a simulation model semiconductor integrated circuit at pc	20021024	716/5	
US 20020063987 A1		Read/write system with reduced write-to-read transition recovery time independent from input	20020530	360/66	
US 20020011885 A1		Power model for EMI simulation to semiconductor integrated circuit, method of designing the	20020131	327/158	
US 6721117 B2		Read/write system with reduced write-to-read transition recovery time independent from input	20040413	360/66	
US 6617910 B2		Low noise analog multiplier utilizing nonlinear local feedback elements	20030909	327/359	
US 6615394 B2		Method and apparatus for preparing a simulation model for semiconductor integrated circuit a	20030902	716/5	
US 6204710 B1		Precision trim circuit for delay lines	20010320	327/276	
US 6174067 B1		Lighting system, apparatus, and method	20010116	362/101	
US 6110219 A		Model for taking into account gate resistance induced propagation delay	20000829	716/1	
US 5790017 A		Vehicle turn signal control system and method	19980804	340/475	
US 5774358 A		Method and apparatus for generating instruction/data streams employed to verify hardware in	19970610	716/5	
US 5638294 A		Device and method for calculating delay time	19960903	703/14	
US 5553008 A		Transistor-level timing and simulator and power analyzer	19960820	703/6	
US 5548539 A		Analysis mechanism for system performance simulator	19960702	714/55	
US 5533197 A		Method to assess electromigration and hot electron reliability for microprocessors	19950829	703/19	
US 5446676 A		Transistor-level timing and power simulator and power analyzer	19930921	703/14	
US 5247468 A		System for calculating and displaying user-defined output parameters describing behavior of ;	19930413	716/5	
US 5202841 A		Layout pattern verification system	19930413	324/537	
US 5202639 A		Method and apparatus for testing analogue circuits	19920714	706/40	
US 5130563 A		Optoelectronic sensory neural network	19920128	716/11	
US 5084824 A		Simulation model generation from a physical data base of a combinatorial circuit	19910917	333/81R	
US 5049841 A		Electronically reconfigurable digital pad attenuator using segmented field effect transistors	19880705	323/289	
US 4755741 A		Adaptive transistor drive circuit	19711207	340/462	
US 3626367 A		VEHICLE SUBSYSTEM MONITORS	20010112		
JP 2001005842 A		DEVICE AND METHOD FOR SIMULATING ELECTRIC CIRCUIT			
NN901082		Voltage-Controlled Oscillator.	19901001		

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☐ Check to search within this result set
**Results Key:****JNL** = Journal or Magazine   **CNF** = Conference   **STD** = Standard**1 A bandpass sigma-delta modulator employing micro-mechanical resonator***Wang, X.; Xu, Y.P.; Wang, Z.; Liw, S.; Sun, W.H.; Tan, L.S.;*

Circuits and Systems, 2003. ISCAS '03. Proceedings of the 2003 International Symposium on , Volume: 1 , 25-28 May 2003

Pages:I-1041 - I-1044 vol.1

[\[Abstract\]](#)   [\[PDF Full-Text \(293 KB\)\]](#)   IEEE CNF
**2 Distributed SPICE circuit model for ceramic capacitors***Smith, L.D.; Hockanson, D.;*

Electronic Components and Technology Conference, 2001. Proceedings., 51st May-1 June 2001

Pages:523 - 528

[\[Abstract\]](#)   [\[PDF Full-Text \(324 KB\)\]](#)   IEEE CNF
**3 Load speed observer-based fuzzy auto-tuning implementation for A speed servo system with two-mass mechanical motion system-experimental verification***Yoshitsugu, J.; Inoue, K.; Nakaoka, M.;*

Industry Applications Conference, 1999. Thirty-Fourth IAS Annual Meeting. Conference Record of the 1999 IEEE , Volume: 1 , 3-7 Oct. 1999

Pages:645 - 652 vol.1

[\[Abstract\]](#)   [\[PDF Full-Text \(328 KB\)\]](#)   IEEE CNF
**4 Analysis and design of AC servo motion drive control system with 2 mass mechanical resonant load***Inoue, K.; Nakaoka, M.;*

Advanced Motion Control, 1996. AMC '96-MIE. Proceedings., 1996 4th International Workshop on , Volume: 2 , 18-21 March 1996  
Pages:600 - 605 vol.2

[[Abstract](#)] [[PDF Full-Text \(496 KB\)](#)] IEEE CNF

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**5 Suppression of flicker in an arc-furnace supply system by an active capacitance-a novel voltage stabilizer in power systems**

*Nabae, A.; Yamaguchi, M.;*

Industry Applications, IEEE Transactions on , Volume: 31 , Issue: 1 , Jan.-Feb. 1995

Pages:107 - 111

[[Abstract](#)] [[PDF Full-Text \(352 KB\)](#)] IEEE JNL

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**6 SAW impedance elements**

*Plessky, V.P.;*

Ultrasonics, Ferroelectrics and Frequency Control, IEEE Transactions on , Volume: 42 , Issue: 5 , Sept. 1995

Pages:870 - 875

[[Abstract](#)] [[PDF Full-Text \(352 KB\)](#)] IEEE JNL

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**7 Estimation of anti-resonance frequencies by using an over-determined high-order Yule-Walker equation**

*Yanagida, M.; Kakusho, O.;*

Acoustics, Speech, and Signal Processing, IEEE International Conference on ICASSP '86. , Volume: 11 , Apr 1986

Pages:601 - 604

[[Abstract](#)] [[PDF Full-Text \(112 KB\)](#)] IEEE CNF

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